

Name: B.KOTESWAR RAO , M.Tech (Ph.D)

Highest Qualification : Pursuing Ph.D in JNTU

Hyderabad

Specialization: Electronics and Communication Engineering.

Experience: 14 years

As a Gate trainer : 2 years

Subject handled in gate : digital circuits

Designation: Associate Professor

E-mail ID: bonagirikoteswarrao@gmail.com

Mobile Number: 9700941151

RESUME

B.KOTESWAR RAO

D.No:6-1-7/10/3/1

Cheruvu Bazar ,
Khammam-507001

E-Mail: bonagirikoteswarrao@gmail.com

Mobile No: 9700941151

Objective

To seek a challenging position and be a part of the Organization where all my capabilities and skills can be utilized for the growth of the organization and myself.

Professional Experience: 14 years

- Worked as a Asst.Prof in ECE dept. of Anurag Engineering college Engineering from 2006 to 2009 (**3 years**)
- Worked as Asst Professor in ECE dept. of Swarna Bharathi College of Engineering from 2009 to 2015 (**6 years**)
- Worked as Asst Professor in ECE dept. of Laqshya Institute of Technology and Science from 2015 to 2016 (**1 years**)
- Worked as a Gate Trainer at Grace Engineering Academy in Khammam from 2014 to 2016 (**2 years**)
- Working as Associate Professor in ECE dept. of Marri Laxman Reddy Institute of Technology and Management since 2016 to till date.

Educational Qualification

- **M.Tech.** in **ECE** with **73.2%** from MADHIRA INSTITUTE OF TECHNOLOGY AND SCIENCE(MITS) affiliated to JNTUH.
- **B.Tech** in **Electronics and Communication Engineering** with **61%** from NMR ENGINEERING COLLEGE Affiliated to JNTUH.
- **Intermediate** with **87.4%** from Baby Moon junior college in Khammam.
- **SSC** with **78.5%** from St.Marys High School in Khammam.

Achievements

- **Ratified by JNTUH** as Assistant Professor.
- Paper published in MICROPROCESSORS AND MICROSYSTEMS on “ **Low area FPGA implementation of modified histogram estimation architecture with CSAC-DPROM-OBC** ” (**SCI JOURNAL**)
- Paper published in International Journal of pure and Applied mathematics on “ **Design and Implementation of 4-Bit Multiplier using Fault Tolerant Self Repairing Full Adder** ” (**SCOPUS FREE JOURNAL**)
- Paper published in International Journal of Engineering and Technology on “ **Smart Water Quality Monitoring System using IoT Technology** ” (**SCOPUS FREE JOURNAL**)
- Paper published in Journal of Advanced Research in Dynamic and control systems on “**Analyze the Face Tracking System Using Shape from Shading Using Image Processing**” (**SCOPUS FREE JOURNAL**)
- Paper published in Journal of Engineering and Advanced Technology on “**Human Face Identification based on Optimal sparse Features**”(**SCOPUS PAID JOURNAL**)
- Paper published in International Journal of Research in Engineering and Applied Sciences on “ **Full Custom Implementation Of An 8b/10b Encoder With A Modified Coding Table**”
- Paper published in International Journal of Research in Engineering and Applied Sciences on “**Microcontroller Based Electronic Visitors Guide**”
- Paper published in International Journal of electronics and communication technology on “**Walking stick with heart attack detection** ”
- Paper published in International Journal of computers and communication technology on “**Real time embedded face recognition using ARM 7** ”
- Paper published in International Journal of computational engineering research on “**Automatic sound profile switching in mobile phones** ”
- Participated in a workshop on “**HIGH IMPACT TEACHING SKILLS**” conducted by DALE CARNEGIE & ASSOCIATES,INC.TRAINER AND WIPRO.

Subjects taught (for B.Tech & M.Tech)

- Electronic Devices and Circuits
- Pulse And Digital Circuits
- Electronic Circuits
- Integrated Circuit Applications
- Microprocessor And Microcontrollers
- Telecommunication and Switching Systems
- Switching Theory and Logic Design
- Computer Organisation
- Analog Communications
- Basic Electrical And Electronic Circuits

M.Tech Project Profile

Title: Full Custom Implementation Of An 8b/10b Encoder With A Modified Coding Table

Description:

This paper presents a design of 8B/10B encoder with a modified coding table. The proposed encoder has been designed based on a reduced coding table with a modified disparity control block. After being synthesized using CMOS 0.18 μ m process, the proposed encoder shows the operating frequency of 343 MHz and occupies the chip area of 1886 μ m² with 189 logic gates. It consumes 2.74mW power. Compared to conventional approaches, the operating frequency is improved by 25.6% and chip area is decreased to 43%.

Personal Information

Name : B.KOTESWAR RAO
Father's Name : Arjuna rao.
Date of Birth : 1-10-1984.
Gender : Male.
Marital status : Married
Nationality : Indian.
Languages Known : English, Telugu and Hindi.
Hobbies : Reading books & Playing Cricket .

Declaration

I here by declare that the information furnished above is true to the best of my knowledge and belief.

Place :

Date :

(B.KOTESWAR RAO)