Curriculum Vitae

Dr. G. AMARNATH **B.Tech, M.Tech, Ph.D.**
Dept. of Electronics & Communication Engineering
Marri Laxman Reddy Institute of Technology & Management
Dundigal, Hyderabad, 500043, India.
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Education

Ph.D.	**National Institute of Technology, Silchar** **SpecialisationAreas:**Semiconductor Device Modeling and Simulation, III-V Compound Semiconductor based-HEMT/MODFET,Microelectronics & VLSI Design. **Supervisor:** Dr. Trupti Ranjan Lenka. **Thesis Title:**Modeling and simulation of AlInN/GaN MOSHEMT formillimeter wave electronic applications.	Awarded on 05-Feb-2019
M.Tech (VLSI SD)	**Jawaharlal Nehru Technological University- Hyderabad**	2007-2009
B.Tech (E.C.E.)	**Jawaharlal Nehru Technological University-Hyderabad**	2003-2007
10+2 (M.P.C.)	**Board of Intermediate Education- Andhra Pradesh** *(Millennium Junior College-Karimnagar)*	2001-2003
SSC	**Board of Secondary Education- Andhra Pradesh** *(Sri Rama Vidyaniketan-Godavarikhani)*	2001

Professional Experience

Total **13+ years of experience** in academics and industry including Ph.D. duration.

Academics	**Marri Laxman Reddy Institute of Technology & Management** Role: *Associate Professor and Associate Dean (R&D)*	Apr 2018 – Till Date
Academics	**National Institute of Technology, Silchar** Role: *Research Scholar and Teaching Assistant*	Jan 2013 – Apr 2018
Industry	**Kacper Technologies, Banglore** Role: *Design & Verification Engineer*	Apr 2012 – Dec 2012
Academics	**Vivekananda Institute of Technology & Sciences, Karimnagar** Role: *Assistant Professor*	Jul 2010 – Mar 2012
Academics	**Sindhura College of Engineering & Technology, Godavarikhani** Role: *Assistant Professor*	Oct 2008 – May 2010

Major Area of Interest

- Microelectronics & VLSI Design,
- SemiconductorMaterials and Physics,
- Modelling and Simulation of Devices,
- VLSI Technology,
- VLSI Design & Verification (Verilog, VHDL, SV, OVM, & UVM)

Funding Projects

Project Title	Scheme	Funding Agency	Status	File Number & Date	Amount (in Rupees)
Agri Innovation Hub for Development of Scheduled Tribe (ST) Community in Narsampet Block, Warangal District, Telangana State	STI-HUB	SEED-DST	Ongoing	DST/SEED/TSP/STI/2020/312	2,98,67,113/-
Exploring Science Communication in Children's of Dundigal and Surrounding villages of Medchal District, Telangana State through Children Centric Outreach Programme	CHILDREN CENTRIC OUTREACH PROGRAMME	NCSTC-DST	Ongoing	CO/B/OR/2021/31 Submitted on 15/03/2021	16,86,960
Nonlinear Modeling and Statistical Analysis of High-Speed Interconnect Systems with Artificial Neural Networks	SRG	SERB	Accepted for Evaluation	SRG/2021/002192/ES Submitted on 02/03/2021	25,93,155
Artificial Intelligence: Devices to Circuits	STTP	AICTE	**Completed**	34-66/90/FDC/STTP/Policy-1/2019-20	2,71,667

Text Books/ Book Chapter

[1] D. K. Panda, **G. Amarnath**, and T. R. Lenka, "*15. Metal Oxide Semiconductor High Electron Mobility Transistors*," in Handbook for III-V High Electron Mobility Transistor Technologies, 1st Edition, 2019, CRC Press, Taylor & Francis. ISBN 978-1-13-862527-3.

[2] G. Amarnath, "*Analytical Modelling of Electric Field and Breakdown-Voltage Characteristics of AlInN/GaN HEMT with Field-Plates*" in HEMT Technology and Applications, Springer, 2022.

[3] **G. Amarnath** and K. Nagabhushanam, "*Electronic Devices and Circuits*" 1st Edition, 2018, Spectrum Techno Press, ISBN 978-93-83470-11-2.

Research Publications

International Journals

[1] **Amarnath, G**., Sharmila, V., Sreenivasulu, Y. et al. AlInN/GaN HEMT on Silicon Substrate with GD-Field-Plate: Modelling and Simulation of Electric-Field and Breakdown-Voltage Characteristics. Silicon (2022). (**SCI, Scopus, Web of Science**)

[2] **G. Amarnath**, D. K. Panda, T. R. Lenka, "Modeling and simulation of DC and microwave characteristics in AlInN(AlGaN)/AlN/GaN MOSHEMTs with different gate length," ***International Journal of Numerical Modelling: Electronic Networks, Devices and Fields***. vol. 32, no. 1, pp. e2456, Jan/Feb. 2019. doi: 10.1002/jnm.2456. (**SCI, Scopus, Web of Science**)

[3] **G. Amarnath**, D. K. Panda, T. R. Lenka, "Microwave frequency small-signal equivalent circuit parameter extraction for AlInN/GaN MOSHEMT," ***International Journal of RF and Microwave Computer-Aided Engineering,*** vol. 28, no. 2, pp. e21179, Feb. 2018. doi: 10.1002/mmce.21179. (**SCI, Scopus, Web of Science**)

[4] **G. Amarnath**, R. Swain, T. R. Lenka, "Modeling and simulation of 2DEG density and intrinsic capacitances in AlInN/GaN MOSHEMT," ***International Journal of Numerical Modelling: Electronic Networks, Devices and Fields,*** vol. 31, no. 1, pp. e2268, Jan. 2018. doi: 10.1002/jnm.2268. (**SCI, Scopus, Web of Science**)

[5] **G.Amarnath**and T. R. Lenka, "Analytical model development for unified 2D electron gas sheet charge density of AlInN/GaN MOSHEMT," ***International Journal of Electronics and Telecommunications***, vol. 63, no. 4, pp. 363-368. Sep. 2017. doi: 10.1515/eletel-2017-0049. (**ESCI, Scopus, Web of Science**)

[6] **G. Amarnath** and T. R. Lenka, "Modeling and simulation of DC and microwave characteristics in AlInN(AlGaN)/AlN/GaN MOSHEMTs with different gate length," ***International Journal of Numerical Modelling: Electronic Networks, Devices and Fields***. (***Accepted for Publication***) **(SCI, Scopus, Web of Science)**

[7] D K Panda, **G. Amarnath**, T R Lenka, "Small-signal model parameter extraction of E–mode n-polar GaN MOS-HEMT using optimization algorithms and its comparison," ***Journal of Semiconductors***, vol. 39, no. 7, July 2018. doi: 10.1088/1674-4926/39/7/074001. **(ESCI, Scopus, Web of Science)**

[8] K. Naresh, **G.Amarnath**, B. Sujatha and K.Srinivasa Rao, "Implementation of low-cost novel RTL modeling of spectrum sensing in cognitive radio networks," ***International Journal of Pure and Applied Mathematics***, vol. 117, no. 19, pp.189-195, 2017.

[9] B Prashanth Kumar, **G.Amarnath,** G S Rao, Wasim Arif, Srimanta Baishya, "Gate Capacitance Extraction, Two Dimensional T- Shaped Junction less Transistor Using Sentaurus TCAD," ***International Journal of Innovative Research in Science, Engineering and Technology***, Special Issue ICIET 2014, No.149, Mar. 2014.

Conferences

[1] D. Sudha, G. Amarnath and V. A, "Utilizing Analog Circuits by Neural-Network based Multi-Layer-Perceptron," 2021 International Conference on Innovative Computing, Intelligent Communication and Smart Electrical Systems (ICSES), Chennai, India, 2021, pp. 1-4. doi: 10.1109/ICSES52305.2021.9633958

[2] G. Amarnath, V. A and D. Sudha, "Noise and IM3 Harmonics Cancelling in Two-Stage Wideband Differential LNA," 2021 Fourth International Conference on Electrical, Computer and Communication Technologies (ICECCT), Erode, India, 2021, pp. 1-4. doi: 10.1109/ICECCT52121.2021.9616845

[3] G. Amarnath, S. Akula and V. A, "Employing Analog Circuits by Neural-Network based Multi-Layer-Perceptron," 2021 Fourth International Conference on Electrical, Computer and

Communication Technologies (ICECCT), Erode, India, 2021, pp. 1-3. doi: 10.1109/ICECCT52121.2021.9616860

[4] G. Amarnath, V. A and B. S. Rao, "Artificial Neural Network Based Statistical-Analysis of High-Speed-Interconnect-Systems," 2021 Fourth International Conference on Electrical, Computer and Communication Technologies (ICECCT), Erode, India, 2021, pp. 1-4. doi: 10.1109/ICECCT52121.2021.9616638

[5] G. Amarnath, S. Vallem and B. S. Rao, "Threshold-Voltage Analytical-Model Development for Junction-less-Double-Gate FETs," 2021 International Conference on Computer Communication and Informatics (ICCCI), Coimbatore, India, 2021, pp. 1-4. doi: 10.1109/ICCCI50826.2021.9402278

[6] G. Amarnath, D. Krishna and A. Vinod, "TCAD-based Comparative Study of Gallium-Oxide based FinFET and MOSFET," 2020 IEEE International Conference on Advent Trends in Multidisciplinary Research and Innovation (ICATMRI), Buldhana, India, 2020, pp. 1-4. doi: 10.1109/ICATMRI51801.2020.9398440

[7] G. Amarnath, D. Sudha, D. Krishna, S. Karthik, S. Ghanate and A. Vinod, "Developement of Threshold-Voltage Analytical-Model for Double-Gate-Junction-less FETs," 2020 IEEE International Conference on Advent Trends in Multidisciplinary Research and Innovation (ICATMRI), Buldhana, India, 2020, pp. 1-5. doi: 10.1109/ICATMRI51801.2020.9398504

[8] G. Amarnath, D. Sudha and S. K. Hima Bindhu, "Analysis of Temperature Effect on Small-Signal-Equivalent-Circuit Parameters for AlInN/GaN MOS-HEMT," 2020 IEEE International Conference on Advent Trends in Multidisciplinary Research and Innovation (ICATMRI), Buldhana, India, 2020, pp. 1-4. doi: 10.1109/ICATMRI51801.2020.9398378

[9] G. Amarnath, D. Sudha, D. Krishna, S. Ghanate, S. Karthik and A. Vinod, "Analytical Model Development for Channel Potential in Junction-less Double-Gate FETs," 2020 IEEE International Conference on Advent Trends in Multidisciplinary Research and Innovation (ICATMRI), Buldhana, India, 2020, pp. 1-5. doi: 10.1109/ICATMRI51801.2020.9398468

[10] G. Amarnath, G. Srinivas and T. R. Lenka, "374GHz cut-off frequency of ultra thin InAlN/AlN/GaN MIS HEMT," 2015 International Conference on Computer Communication and Informatics (ICCCI), Coimbatore, India, 2015, pp. 1-4. doi: 10.1109/ICCCI.2015.7218141

[11] G. Amarnath, G. Srinivas and T. R. Lenka, "Electrical characteristics and 2DEG properties of passivated InAlN/AlN/GaN HEMT," 2015 International Conference on Computer Communication and Informatics (ICCCI), Coimbatore, India, 2015, pp. 1-4. doi: 10.1109/ICCCI.2015.7218142

[12] K. Dharavath, G. Amarnath, F. A. Talukdar and R. H. Laskar, "Impact of image preprocessing on face recognition: A comparative analysis," 2014 International Conference on Communication and Signal Processing, Melmaruvathur, India, 2014, pp. 631-635. doi: 10.1109/ICCSP.2014.6949918

[13] B. P. Kumar, G. Amarnath, W. Arif and S. Baishya, "An improved gate capacitance for two dimensional junctionless transistor," 2014 International Conference on Green Computing Communication and Electrical Engineering (ICGCCEE), Coimbatore, India, 2014, pp. 1-3. doi: 10.1109/ICGCCEE.2014.6922275

[14] D. Sudha, and G. Amarnath, “Developement of an Analytical-Model for Channel-Potential in Junction-less-Double-Gate FETs,” International Conference on Intelligent Computing and Applications (ICICA 2020), December 22nd-24th, 2020, Keonjhar, Odisha. “Advances in Intelligent Systems and Computing” (AISC).

[15] G. Amarnath, Manisha Guduri, Vinod A, and M. Kavicharan, “Study of Temperature Effect on MOS-HEMT Small-Signal Parameters,” International Conference on Micro/Nanoelectronics Devices, Circuits and Systems (MNDCS-2021), 30-31 Jan 2021, Silchar, Assam. “Lecture Notes in Electrical Engineering (LNEE)” series.

[16] G. Amarnath, Manisha Guduri, Vinod A, and M. Krishnasamy, “Numerical Simulation based Comparative Study of FinFET and MOSFET with Gallium-Oxide,” International Conference on Micro/Nanoelectronics Devices, Circuits and Systems (MNDCS-2021), 30-31 Jan 2021, Silchar, Assam. “Lecture Notes in Electrical Engineering (LNEE)” series.

[17] Jagritee Talukdar, G. Amarnath and M. Kavicharan, “Flicker noise analysis of Non-uniform body TFET with dual material source (NUTFET-DMS),” International Conference on

Micro/Nanoelectronics Devices, Circuits and Systems (MNDCS-2021), 30-31 Jan 2021, Silchar, Assam. “Lecture Notes in Electrical Engineering (LNEE)” series.

[18] M. Krishnasamy, Jitesh Ramdas Shinde, H P Mohammad, G. Amarnath and T. R. Lenka, “Design and Analyze of FEM novel X-Shaped Broadband Linear Piezoelectric Energy Harvester,” International Conference on Micro/Nanoelectronics Devices, Circuits and Systems (MNDCS-2021), 30-31 Jan 2021, Silchar, Assam. “Lecture Notes in Electrical Engineering (LNEE)” series.

[19] K Girija Sravani, N. Yashwont Sai, M. Billscott, P. Gowtham Reddy, Sharmila Vallem, G. Amarnath and K. Srinivasa Rao, “Design and Simulation of RF MEMS Capacitive Contact Shunt Switch for S-band Application,” International Conference on Micro/Nanoelectronics Devices, Circuits and Systems (MNDCS-2021), 30-31 Jan 2021, Silchar, Assam. “Lecture Notes in Electrical Engineering (LNEE)” series.

[20] K Srinivasa Rao, B.S.D. Karthik Raja, Ch. Manisai, M. Tharun Sai Reddy, Biyyani Srinivasa Rao and G. Amarnath, “Design and Simulation of High-Performance Full Adder Using 6-T XOR–XNOR Cell,” International Conference on Micro/Nanoelectronics Devices, Circuits and Systems (MNDCS-2021), 30-31 Jan 2021, Silchar, Assam. “Lecture Notes in Electrical Engineering (LNEE)” series.

[21] K Srinivasa Rao, B. Uday Teja, A. Sai Harish, B. Aravind, Sharmila Vallem and G. Amarnath, “Analysis of ALU Using Reversible Gates in Verilog,” International Conference on Micro/Nanoelectronics Devices, Circuits and Systems (MNDCS-2021), 30-31 Jan 2021, Silchar, Assam. “Lecture Notes in Electrical Engineering (LNEE)” series.

[22] G.Amarnath, G.Srinivas and T R Lenka, “Comparative study of InAlN/GaN based HEMT and MOSHEMT with AlN spacer layer,” *Proceedings of International Symposium on Semiconductor Materials and Devices (ISSMD-3),* 2-5 Feb. 2015.

[23] G.Amarnath and T R Lenka, “Polarization induced 2DEG characteristics of strained InAlN/GaN-based HEMT,” *Proceedings of International Symposium on Semiconductor Materials and Devices (ISSMD-3),* 2-5 Feb. 2015.

[24] G.Amarnath, G.Srinivas and T R Lenka, “Electrical characteristics and 2DEG properties of passivated InAlN/AlN/GaN HEMT,” *International Conference on Computer Communication and Informatics (ICCCI -2015),* 08 – 10 Jan. 2015.*(IEEE Xplore)*

[25] G.Amarnath, G.Srinivas and T R Lenka, “374 GHz Cut-Off frequency of ultra thin InAlN/AlN/GaN MISHEMT,” *2015 International Conference on Computer Communication and Informatics (ICCCI -2015),* 08 – 10 Jan 2015.*(IEEE Xplore)*

[26] R. Swain, K. Jena, A. Gaini, TR Lenka, "Comparative study of AlN/GaN HEMT and MOSHEMT structures by varying oxide thickness," *2014 IEEE 9th Nanotechnology Materials and Devices Conference (NMDC),* pp.128-131, 12-15 Oct. 2014.*(IEEE Xplore)*

[27] D Krishna, G Amarnath, F A Talukdar, R H Laskar, "Impact of image preprocessing on face recognition: A comparative analysis," *International Conference on Communications and Signal Processing(ICCSP),* pp.631-635, 3-5 Apr2014.*(IEEE Xplore)*

[28] B P Kumar,G Amarnath, W Arif, S Baishya, "An improved gate capacitance for two dimensional junction less transistor," *International Conference on Green Computing Communication and Electrical Engineering,* pp.1,3, 6-8 Mar 2014.*(IEEE Xplore)*

[29] G.Amarnath and T R Lenka “Comparative study on DC characteristics of AlGaN/GaN and AlInN/GaN HEMTs,” *International Conference on Physics of Semiconductor Devices*,Noida, 10-13 Dec 2013.

[30] G.Amarnath and T R Lenka “Review of GaN HEMTs for high frequency performance,”*International Conference on Advances in Computer Science,* NCR, India, 13-14 Dec 2013.

[31] Amarnath Gaini, and K Saritha, “Design and implementation of blowfish encryption algorithm” *RITS International Conference on Advancements in Engineering & Management,* Hyderabad, 28-29 Feb 2012.

[32] Amarnath Gaini, and K Saritha, "Memory hierarchies, pipelines, and buses for future architectures in time-critical embedded systems" *RITS International Conference on Advancements in Engineering & Management,* Hyderabad, 28-29 Feb 2012.

[33] Gaini Amarnath, and K Saritha; "64-bit block cipher encryption algorithm for information security"*International Conference on Information Systems Security,* Gandhinagar, India, 17-19, Dec 2010.

[34] Amarnath Gaini, "SOC design for blowfish cryptographic Algorithm" *National Conference on Recent Advancements in Communication & Electronics,* KITS-Huzurabad, 2011.

[35] Amarnath Gaini, M Vijayalaxmi, "Blowfish encryption algorithm for text and image with chaos based S-box"*National conference on Assistive Technology, BVRIT-Narsapur,* 29-31July 2011.

[36] Amarnath Gaini, "Analyzing hardware-software requirement errors in co-synthesis for embedded systems", *National conference on Assistive Technology, BVRIT-Narsapur,* 29-31 July 2011.

Professional Membership Details

- IEEE – Member IEEE (2013 to present) : 92747970
- Student Member, IEEE Electron Devices (ED) Society-USA – (S'13)
- MISTE - Life Member of I.S.T.E: LM76919
- International Association of Engineers (IAENG): 240137

Award/Grant/Fellowship:

- Research Fellowship during Ph.D.from MHRD, Govt. of India.
- Financial support from TEQIP-II to attend Familiarization workshop on IC fabrication and characterization process at IIT Bombay under the scheme of Indian Nano-technology User Program (INUP) in Dec-2013.
- Financial grant from TEQIP-IIfor fabrication and characterization of devie at IISc.Banglore under the scheme of Indian Nano-technology User Program (INUP) in June-2014.
- Travel Grant from NIT-Silchar and TEQIP-II to present research papers in various conferences and workshops.

Additional Training

- Wipro Mission10XCertification for High impact Teaching & Learning Methodology.
- INUP Hands-on Training onNanoelectronics Fabrication technologies at IIT-Bombay
- INUP familiarization workshop and Hands-on Training on clean room fabrication facility and Preparation of micro/nano scale device at IISc-Banglore.
- Agilent ADS Tool Training on RF, microwave, and high speed digital applications at NIT-Silchar.
- Silvaco TCAD tool training on Process and Device simulation at NIT-Silchar.
- GIAN course on "Nanoelectronics Challenges for Internet of Things" organized by Dept. of ECE, NIT Silchar and MHRD, Govt. of India from 5th to 9th January 2017..
- GIAN course on "Mapping algorithms to VLSI architectures" during August 1-5, 2016 organized by Dept. of ECE and MHRD, Govt. of India.

❖ Attended various FDPs, workshops, Symposiums, and Conferences which are relevant to research areas.

Personal Profile

Name	:	Amarnath Gaini
Father's Name	:	Mallaiah
Mother's Name	:	Radha
Marital Status	:	Married

Date of Birth	:	20-05-1986
Languages Known	:	English, Telugu & Hindi
Permanent Address	:	H.NO:16-3-49, L.B.Nagar, Godavarikhani-505209, Peddapalli (Telangana).

(Amarnath Gaini)