Dr. Kishore Sanapala, M.Tech., Ph.D.
Associate Professor,
Dept. of Electronics and Communication Engineering,
MLRITM, Hyderabad-500043, India.
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Objective:

To achieve high career growth through the continuous learning process and keep myself dynamic, visionary, and competitive with the changing scenario of technology.

Research Interests:

- Subthreshold/Near threshold digital design for Ultra Low Power Applications.
- Low Power library cell design- GDI.
- Near Zero Computing circuits for IoT and ML networks.

Skill Set:

- **Cadence Tool**: Schematic to GDSII; Virtuoso Schematic Editor, Virtuoso ADE, Virtuoso Spectre Circuit simulator, Virtuoso Layout Suite (DRC, LVS, xRC).
- **Syopsis Tool:** Custom Compiler, PrimeSim SPICE- PrimeWave Design Environment.
- **Mentor Graphics Tool:** Pyxis Schematic Editor, Eldo Simulator, EZwave, Calibre (DRC, LVS).
- **Others:** Xilinx ISE (RTL using HDL), Tanner EDA, ORCAD, Microwind.

Education Details:

- **Ph.D (2015-2019)**: Ph.D thesis titled "Energy Efficient Ultra Low Voltage Techniques for Adder and SRAM Circuits" under the supervision of Dr. Sakthivel R, Associate professor, Dept. of Micro & Nanoelectronics, School of Electronics Engineering, VIT University, Vellore, India.

  Thesis Brief: Scaling down the supply voltage towards the subthreshold/near-threshold operation is one of the prominent solutions for energy efficient applications because it often provides the minimum energy per operation. Various contributions were made with the design of full adder and SRAM circuits that allows the circuit designers more reachable to the subthreshold design. Performance of various body bias schemes were analysed. The performance of all the proposed circuits with post layout simulations is analysed across different process corners and supply voltages using 45nm technology in Cadence tool.

- **M.Tech (2012-2014):** VLSI Design from Sathyabama University (with 1st class –Distinction, 7.7 GPA), Chennai, India.
- **B.Tech (2008-2012):** Electronics & Communication Engineering (ECE) from JNTUK (with 1st class, 65.31%), Kakinada, India.
- **Intermediate (2006-2008):** MPC, Board of Intermediate education (with 85.8%), Andhra Pradesh.
- **S.S.C:** Board of Secondary education (with 86.16%), Andhra Pradesh.

Academic Appointments Held: Total work Experience- 7 Years

- **Associate Professor:** From July-2019 to present, MLRITM, Hyderabad.
- **Assistant Professor:** From July-2018 to July-2019 (1 Year), Presidency University, Bangalore.
- **Research Associate**: From June-2015 to June-2018 (3 years) at VIT University, Vellore.
- **Assistant Professor**: From June-2014 to May-2015 (1year) at VITS college of Engineering, Visakhapatnam.

Refereeing:

- Microelectronics Journal- Elsevier
- International Journal of Electronics (Taylor & Francis)
- IET Computers and Digital Techniques Journal
- International Journal of Systems of Systems Engineering- Inderscience
- Journal of Engineering Science & Technology
- Gazi University Journal of Science
- ICMDCS-2017 IEEE International conference, VIT-Vellore, India
- SNSP-2019 Springer International conference, Hualien, Taiwan
- ISES-2020 IEEE International conference, VIT, Chennai, India
- INDISCON-2020 IEEE International Conference, GVPCE, Visakhapatnam, India.

Publications:

Journal Articles:

- Thaseen IS, Mohanraj V, Ramachandran S, **Kishore Sanapala**, Yeo S-S. A Hadoop Based Framework Integrating Machine Learning Classifiers for Anomaly Detection in the Internet of Things. *Electronics*. 2021; 10(16):1955. (Indexed in Scopus, Thomson Reuters-SCI; SNIP=1.014; IF=2.4).

- **Kishore Sanapala**, Satyanarayana S.V.V, Sakthivel R, "Near-zero Computing using NCFET for IoT applications", International Journal of Intelligent Enterprise, Inderscience, Published online in the forthcoming articles, July -2020. (Indexed in Scopus, SNIP=0.8).

- G. Nagajyothi, **Kishore Sanapala,** A. Vijalakshmi, "ASIC Implementation of Distributed Arithmetic based FIR Filter Using RNS for High Speed DSP Systems", Journal of Speech Technology, Springer, 23(2), February 10th - 2020. (Indexed in Scopus, Thomson Reuters-ESCI; SNIP=1.4).

- **Kishore Sanapala**, and Sakthivel R, "Ultra-Low Voltage GDI based Hybrid Full Adder Design for Area and Energy Efficient Computing Systems", IET Circuits Devices & Systems 13(4), Jan-2019. (Indexed in Scopus, Thomson Reuters-SCI; SNIP=1.014; IF=1.395).

- **Kishore Sanapala,** Sakthivel R, S.S. Yeo "Schmitt Trigger Based Single Ended SRAM Cell for IoT Applications", Journal of Supercomputing, Springer, 74(9), May-2018. (Indexed in Scopus, Thomson Reuters-SCI; SNIP=1.17; IF=2.469).

- **Kishore Sanapala**, Sakthivel R, "Two Novel Subthreshold Logic Families for Area and Ultra low-Energy Efficient Applications: DTGDI & SBBGDI", in Gazi University Journal of Science, 30(4), Dec-2017, pp. 283-292. (Indexed in Scopus, Thomson Reuters ESCI- Web of Science; SNIP= 0.261).

- **Kishore Sanapala**, Sakthivel R, "Design of Full Adder using Subthreshold DTPT Logic", in Advances in Systems Science and Applications, 16(1), Jan-2016, pp. 85-94. (Indexed in Scopus; SNIP= 0.590).

- **Kishore Sanapala,** Sakthivel R, "Low Power Realization of Subthreshold Digital Logic Circuits Using Body Bias Technique", in Indian Journal of Science and Technology, 9(5), Feb-2016, pp. 1-5. (Indexed in Scopus; SNIP= 2.108).

- Sakthivel R, Vanitha M, **Kishore Sanapala,** Thirumalesh K, "Low power modulo 2^n+1 multiplier using data aware adder tree" published in Procedia computer science, Elsevier Journal, volume-70, 2015. (Scopus Indexed, SNIP=0.716).

- **Kishore Sanapala**, K.S.S.D. Madhuri, Mary Sajin Sanju "Exploring CMOS logic families in sub threshold region for ultralow power applications" IOSR Journal of Electrical and Electronics Engineering, 9(1), 2014.

Conferences:

- Prasanna K, **Kishore Sanapala**, and Prabhakar VSV, "Asymmetric and Sector nulling of a linear phased array antenna using Gaussian Mutated Cat Swarm Optimization", 2020 IEEE 5th International Conference on Computing Communication and Automation (ICCCA), Greater Noida, India, (Accepted-Scopus Indexed).

- Prasanna K, **Kishore Sanapala**, and Prabhakar VSV, "Implementation of Sequence Detector using Optimized GDI Technique", 2021 IEEE IAS GUCON, Kuala Lumpur, Malaysia (Accepted-Scopus Indexed).

- V. Chandralekha, L. Navya, **Kishore. Sanapala** and N. Syamala, "Performance Analysis of GDI based Arithmetic Circuits," 2020 IEEE 5th International Conference on Computing Communication and Automation (ICCCA), Greater Noida, India, 2020, pp. 481-485. (Scopus indexed).

- V. Chandralekha, L. Navya, N. Syamala and **Kishore. Sanapala**, "Design of 8 bit and 16-bit Reversible ALU for Low Power Applications," 2020 IEEE 5th International Conference on Computing Communication and Automation (ICCCA), Greater Noida, India, 2020, pp. 477-480. (Scopus indexed)-

- **Kishore Sanapala,** Sakthivel R, "Analysis of GDI Logic for Minimum Energy Optimal Supply Voltage", proceedings of 2017 International Conference on Microelectronic Devices, Circuits and Systems, Vellore, India; included in IEEE Xplore Digital Library. (Scopus indexed).

- **Kishore Sanapala**, Satyanarayana S.V.V, Sakthivel R, "Near-zero Computing using NCFET for IoT applications", proceedings of 2019 International Conference on Advanced Computing and Big Data Analytics, Vellore, India, Mar-2018. (Scopus Indexed).

Book Chapter:

- Dinesh P., Kishore Sanapala., Jyothi G.N., Sakthivel R. (2021) Comparative Review of MAC Architectures. In: Marriwala N., Tripathi C.C., Jain S., Mathapathi S. (eds) Soft Computing for Intelligent Systems. Algorithms for Intelligent Systems. Springer, Singapore.

- **Kishore Sanapala**., Shree L.R., Sakthivel R. (2018) Design of Ultralow Voltage-Hybrid Full Adder Circuit Using GLBB Scheme for Energy-Efficient Arithmetic Applications. In: Anguera J., Satapathy S., Bhateja V., Sunitha K. (eds) Microelectronics, Electromagnetics and

Telecommunications. Lecture Notes in Electrical Engineering, vol 471. Springer, Singapore. (Scopus indexed).

Funding Projects:

Title: Enabling In-Memory Near Zero Computing: CMOS and post-CMOS SRAM Circuits for IoT Applications.

Funding Agency/Scheme: AICTE- RPS

Status: In Evaluation

AQUIS Application ID: 1-9336774123

Amount: 24,32,000

Achievements, Participation in Conferences, Workshops, and Industrial/Academic Training Programmes:

2021

- AICTE Training and Learning (ATAL) online Faculty Development Program on "Systems Engineering" from 21st to 25th July-2021 at MNIT- Bhopal, India.
- Resource Person for the AICTE sponsored STTP on "AI: Devices to Circuits' from 1st to 6th Feb-2021 at MLRITM- Hyderabad, India.

2020

- AICTE Training and Learning (ATAL) online Faculty Development Program on "Quantum Computing" from 15th to 19th June-2020 at NITTR- Chandigarh, India.
- AICTE Training and Learning (ATAL) online Faculty Development Program on "Augmented Reality (AR) and Virtual Reality (VR)" from 15th to 19th June-2020 at UIET, University of Kurukshethra, India.
- Completed 3 online courses specialized on "Strategic Management and Leadership" authorized by University of Illinois at Urbana-Champaign offered through Coursera, dated- 26/06/2020.
- IEEE sponsored online STTP on "An Emerging Paradigm of Low Power Computational VLSI Design" from 16th to 20th june-2020 at BVRIT, Narsapur, Telangana, India.
- Completed online course on "Outcome Based Education (OBE) & Academic Quality Assurance" offered through Udemy, dated- 25/05/2020.

- FDP on “Research Challenges and Opportunities post Covid-19” (RECOP 2020) from 4th to 9th may-2020.

2019

- Awarded with Ph.D for my thesis titled “Energy Efficient Ultra Low Voltage Techniques for Adder and SRAM Circuits” under the supervision of Dr. Sakthivel R, Associate professor, Dept. of Micro & Nanoelectronics, School of Electronics Engineering, VIT University, Vellore, India.

2018, 2017

- Research Award for the year 2017-2018 from VIT-Vellore in recognition for the contribution to research through publication in peer reviewed journals and books.
- International Conference on Advanced Computing and Big Data Analytics, Vellore, India, Mar-2018
- Faculty Development Program on “RTL to GDSII using Cadence EDA Tools” organized by the Dept. of Micro and Nanoelectronics, School of Electronics Engineering (SENSE), VIT University, Vellore, held on 12th &13th January-2018.
- 3rd International Conference on “Micro-Electronics, Electromagnetics and Telecommunications (ICMEET)” held on 9th &10th September-2017 at BVRIT College of Engineering for Women, Hyderabad.
- International Conference on Microelectronic Devices, Circuits and Systems (ICMDCS) held on 10th &12th August-2017 at VIT University, Vellore.
- Faculty Development Program on “Full Custom & Semi Custom IC Design Flow using Synopsis Tool” organized by the Dept. of Micro and Nanoelectronics, School of Electronics Engineering (SENSE), VIT University, Vellore campus, held on 5th & 6th April -2017.
- Global Initiative of Academic Networks (GIAN) course certification (MHRD, India) on "Near/sub-threshold circuits and architectures for microprocessors" organized by Dept. of Electrical Engineering, IIT Madras, held from 9th to 13th January-2017.

2016

- Faculty Development Program on “Analog Electronic Circuits” organized by the Dept. of Micro and Nanoelectronics, School of Electronics Engineering (SENSE), VIT University, Vellore campus, held from 31st May to 4th June-2016.
- 29th international conference on VLSI design and 15th International conference on Embedded Systems (VLSID) held from 4th to 8th January-2016 at Kolkata.

2015

- Verified certificate of achievement in "nano530X: Fundementals of Nanotransistors", a course of study offered by PurdueX, an online learning initiative of Purdue University, U.S.A through edX.

- Faculty Development Program on "Physical Design Flow using Synopsis IC Compiler" organized by the VLSI division, School of Electronics Engineering (SENSE), VIT University, Vellore campus, held on 26th & 27th November-2015.

- One day workshop on "Scientific Writing", organised by Periyar E.V.R.Central Library, VIT University in association with dept.of Library and Information Science, University of Madras, held on 30th Oct-2015 at VIT University Vellore.

- Faculty Development Program on "Simulation of Nanoscale Devices using Synopsis TCAD" organized by the VLSI division, School of Electronics Engineering (SENSE), VIT University, Vellore campus, held on september-2015.

2014, 2013, 2011

- Two-day workshop on "Exploring Entrepreneurship Opportunities" organized by JNTUK, Kakinada, held on 10th &11th October-2014 at Visakhapatnam.

- National Conference on Emerging trends in VLSI, Embedded and Nanotechnologies held on June 2013 and organized by department of ECE, Satyabhama University at Chennai.

- Undergone industry-oriented training at Visakhapatnam Airport, certified by Airports Authority of India (AAI) on "CNS Facilities" from 9th to 27th May-2011.

- Participated in "THE HINDU EDUCATION PLUS" inter & intra collegiate E-PLUS CLUB challenge 2011.

PERSONAL INFORMATION:

- Date of Birth : 11th October 1990.
- Father's name : Late. Sri. S. Visweswara rao.
- Languages known : English, Telugu and Tamil.
- Address : No: 72, Praneeth Pranav Meadows, Bowrampet, Hyderabd-500043.