Course Code: 1930513 Roll No: **MLRS- R19**

MARRI LAXMAN REDDY
INSTITUTE OF TECHNOLOGY AND MANAGEMENT
(AN AUTONOMOUS INSTITUTION)
(Approved by AICTE, New Delhi & Affiliated to JNTUH, Hyderabad)
Accredited by NBA and NAAC with 'A' Grade & Recognized Under Section2(f) & 12(B)of the UGC act,1956

II B.Tech I Sem Regular End Examination, March 2021

COMPUTER ORGANIZATION AND ARCHITECTURE
(CSE)

Time: 3 Hours. **Max. Marks: 70**

Note: 1. Answer any FIVE questions.
2. Each question carries 14 marks and may have a, b as sub questions.

1	a)	Discuss the block diagram of digital computer.	9M	CO2	BL2
	b)	What is the importance of three state buffers?	5M	CO2	BL1
2		Explain the phases of instruction cycle and with a diagram illustrate register transfers for the fetch phase.	14M	CO1	BL2
3	a)	Make a comparison of hardwired control with micro programmed control.	7M	CO2	BL4
	b)	Describe decoding of micro operation fields in control unit.	7M	CO2	BL4
4		Explain Booth algorithm for multiplication of signed-2's complement numbers with an example and necessary flowchart.	14M	CO5	BL2
5	a)	Explain any four instructions used in process control.	7M	CO1	BL2
	b)	Describe the block diagram of BCD adder.	7M	CO5	BL2
6		Why does DMA have priority over the CPU when both request a memory transfer? Explain with illustrations.	14M	CO3	BL4
7	a)	Discuss organization of a 2M X 32 memory module using 512 K X 8 static memory chips with a diagram.	7M	CO3	BL6
	b)	What is cache coherence? Why is it important in shared memory multi processor system? How can the problem be resolved with a snoopy cache controller?	7M	CO4	BL4
8		Discuss the major difficulties that cause the instruction pipeline to deviate from its normal operation and the techniques to overcome them.	14M	CO4	BL2

---oo0oo---