Course Code: 1930513   Roll No: MLRS- R19

MARRI LAXMAN REDDY
INSTITUTE OF TECHNOLOGY AND MANAGEMENT
(AN AUTONOMOUS INSTITUTION)
(Approved by AICTE, New Delhi & Affiliated to JNTUH, Hyderabad)
Accredited by NBA and NAAC with 'A' Grade & Recognized Under Section2(f) & 12(B)of the UGC act,1956

MLRS

II B.Tech I Sem Supplementary Examination, February-2022
Computer Organization and Architecture
(CSE)

Time: 3 Hours.   Max. Marks: 70

Note: 1. Answer any FIVE questions.
      2. Each question carries 14 marks and may have a, b as sub questions.

1	a)	Draw the block diagram of Digital Computer and explain function of each unit.	7M	CO1	U
	b)	Discuss register transfer language concept with examples	7M	CO1	AP
2	a	Explain instruction cycle phases.	7M	CO1	U
	b	Discuss the importance of memory reference instructions in computers with examples	7M	CO1	AP
3	a)	Classify the instructions based on the fields of instruction format.	7M	CO2	U
	b)	Explain about addressing modes with examples.	7M	CO2	AP
4		Illustrate hard wired control unit and micro programmed control unit in detail.	14M	CO2	U
5	a)	Describe Fixed Point and Floating Point number Representation.	7M	CO3	U
	b)	Explain Booth's multiplication algorithm with example.	7M	CO3	AP
6	a)	Explain addition and subtraction in floating point arithmetic.	7M	CO3	U
	b)	Demonstrate the division algorithm	7M	CO3	U
7	a)	Explain block diagram of DMA controller	7M	CO4	U
	b)	Define cache memory? Explain various mapping techniques.	7M	CO4	R
8	a)	Compare RISC and CISC.	7M	CO5	An
	b)	Explain Instruction Pipelining	7M	CO5	U

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