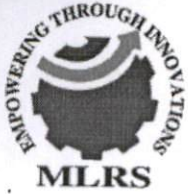


Final: 29-10-21

Course Code: 1930513

Roll No:

MLRS- R19



**MARRI LAXMAN REDDY**  
**INSTITUTE OF TECHNOLOGY AND MANAGEMENT**

(AN AUTONOMOUS INSTITUTION)

(Approved by AICTE, New Delhi & Affiliated to JNTUH, Hyderabad)

Accredited by NBA and NAAC with 'A' Grade & Recognized Under Section 2(f) & 12(B) of the UGC act, 1956

II B.Tech I Sem Supply End Examination, October 2021  
**COMPUTER ORGANIZATION AND ARCHITECTURE**  
(CSE)

Time: 3 Hours.

Max. Marks: 70

Note: 1. Answer any FIVE questions.

2. Each question carries 14 marks and may have a, b as sub questions.

- |   |  |     |     |     |
|---|--|-----|-----|-----|
| 1 | a) Differentiate between computer organization and computer architecture   | 7M  | CO1 | BL5 |
|   | b) Construct a bus system for four registers and explain its function table.   | 7M  | CO1 | BL6 |
| 2 | Explain in detail about arithmetic micro-operations and logic micro-operations.                                      | 14M | CO1 | BL2 |
| 3 | a) What is control memory? Discuss the address sequencing capabilities required in a control memory.                 | 7M  | CO2 | BL1 |
|   | b) Explain the instruction formats in detail.  | 7M  | CO2 | BL2 |
| 4 | Explain addition and subtraction of floating point numbers with an example and necessary flowchart.                  | 14M | CO2 | BL1 |
| 5 | a) What are the various addressing modes followed in instructions? Briefly discuss them.                             | 7M  | CO3 | BL2 |
|   | b) Discuss the hardware for multiplication of two fixed-point binary numbers.  | 7M  | CO3 | BL2 |
| 6 | Design parallel priority interrupt hardware for a system with eight interrupt sources and explain its functionality. | 14M | CO4 | BL6 |
| 7 | a) What are the differences among direct mapping, associative mapping and set associative mapping of cache memory?   | 7M  | CO4 | BL4 |
|   | b) Draw a space time diagram for a six segment pipeline showing the time it takes to process eight tasks.            | 7M  | CO5 | BL6 |
| 8 | What is an array processor? Explain in detail different types of array processors with necessary block diagram.      | 14M | CO5 | BL1 |

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