



# MARRI LAXMAN REDDY INSTITUTE OF TECHNOLOGY AND MANAGEMENT

(AN AUTONOMOUS INSTITUTION)

(Approved by AICTE, New Delhi &amp; Affiliated to JNTUH, Hyderabad)

Accredited by NBA and NAAC with 'A' Grade &amp; Recognized Under Section 2(f) &amp; 12(B) of the UGC act, 1956

II B.Tech I Sem Regular End Examination, March 2021

**DIGITAL SYSTEM DESIGN****(ECE)****Time: 3 Hours.****Max. Marks: 70**

Note: 1. Answer any FIVE questions.

2. Each question carries 14 marks and may have a, b as sub questions.

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|---|---|----|-----|-----|
| 1 | a) Convert the following numbers to required form:<br>i) 197.54 to binary ii) 2035 octal to hexadecimal   | 7M | C01 | BL2 |
|   | b) i) Find the 12 bit 2's compliment of -197.5<br>ii) Generate 12 bit Hamming code for the given 8 bit data word 10111001 that corrects and detects single error. | 7M | C01 | BL2 |
| 2 | a) Simplify the following function: $f(A,B,C) = (A+B)(A+C') + A'B' + A'C'$  | 7M | C02 | BL2 |
|   | b) Prove that NAND and NOR gates are Universal gates  | 7M | C02 | BL2 |
| 3 | a) Simplify the following logic expression using K map:<br>$\Pi M(1,4,5,11,12,14) + D(6,7,15)$  | 7M | C02 | BL2 |
|   | b) Design a 3 bit adder/subtractor logic circuit.   | 7M | C03 | BL3 |
| 4 | a) Describe the Flip-Flop operational characteristics viz. propagation delay time, set-up time, hold time, max clock frequency etc.                               | 7M | C03 | BL3 |
|   | b) Convert a T flip flop to S-R flip-flop   | 7M | C03 | BL3 |
| 5 | a) Design a 4 bit comparator using AND, OR, NOT gates.  | 7M | C03 | BL3 |
|   | b) Draw the timing waveform of 3 bit ripple counter, what is the effect of propagation delay in it, and convert this counter into a ring counter.                 | 7M | C03 | BL3 |
| 6 | a) Design an even parity bit generator using T flip-flops.  | 7M | C03 | BL3 |
|   | b) Design a Modulo-7 counter using J K flip-flops.  | 7M | C03 | BL3 |
| 7 | a) List out the steps in designing a sequential circuit as a Mealy FSM and as Moore's FSM.  | 7M | C03 | BL1 |
|   | b) Compare the basic features of the following logic families: DTL, RTL, TTL and CMOS.  | 7M | C04 | BL2 |
| 8 | a) How are integrated circuits classified? Give brief working of CMOS transmission gate.  | 7M | C04 | BL2 |
|   | b) Explain the process of TTL logic driving the CMOS logic.   | 7M | C04 | BL2 |