Course Code: 1930413 **Roll No:** **MLRS- R19**

MARRI LAXMAN REDDY
INSTITUTE OF TECHNOLOGY AND MANAGEMENT
(AN AUTONOMOUS INSTITUTION)
(Approved by AICTE, New Delhi & Affiliated to JNTUH, Hyderabad)
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II B.Tech I Sem Supplementary Examination, February-2022

Digital System Design

(ECE)

Time: 2 Hours. **Max. Marks: 70**

Note: 1. Answer any FIVE questions.
2. Each question carries 14 marks and may have a, b as sub questions.

Time: 3 Hours. **Max. Marks: 70**

Note: 1. Answer any FIVE questions.
2. Each question carries 14 marks and may have a, b as sub questions.

1	a)	Convert $(A0F9.0EB)_{16}$ to decimal, binary, octal.	7M	CO1	BL2
	b)	Simplify the following Boolean expressions using the Boolean theorems. (i) (A+B+C) (B'+C) + (A+D) (A'+C) (ii) (A+B) (A+B') (A'+B)	7M	CO1	BL1
2		Demonstrate all digital logic gates with truth table.	14M	CO1	BL2
3	a)	Minimize the following expression using K-map and realize using NAND Gates. F (A,B,C,D) = Σm (0,1,2,9,11) +d(8,10,14,15).	7M	CO2	BL2
	b)	Design a combinational circuit by converting BCD code to Excess-3 Code.	7M	CO2	BL3
4		Realize the function f(A,B,C,D)=π(1,4,6,10,14)+d(0,8,11,15) using: i) 16:1 MUX ii) 8:1 MUX.	14M	CO2	BL2
5	a)	Discuss about a D- Latch using NOR gates in detail, with a neat diagram.	7M	CO3	BL1
	b)	Convert an SR Flip-Flop into JK Flip-Flop.	7M	CO3	BL2
6		Design and explain Ring and Johnson counter.	14M	CO3	BL3
7	a)	What is the need of parity generator? Explain with an example.	7M	CO4	BL1
	b)	What are the Moore and Melay machines? Compare them.	7M	CO4	BL2
8		Write a short notes on CMOS logic families	14M	CO5	BL1

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