Course Code: 1930413 Roll No: MLRS- R19

MARRI LAXMAN REDDY
INSTITUTE OF TECHNOLOGY AND MANAGEMENT
(AN AUTONOMOUS INSTITUTION)
(Approved by AICTE, New Delhi & Affiliated to JNTUH, Hyderabad)
Accredited by NBA and NAAC with 'A' Grade & Recognized Under Section2(f) & 12(B)of the UGC act,1956

II B.Tech I Sem Supplementary Examination, July-2022

Digital System Design

(ECE)

Time: 3 Hours. **Max. Marks: 70**

Note: 1. Answer any FIVE questions.
2. Each question carries 14 marks and may have a, b as sub questions.

1	a)	What is the use of complements? Perform subtraction using 10's complement for the given numbers (565)-(666).	7M	CO1	BL1
	b)	Why a NAND and NOR gates are known as universal gates? Simulate all the basic Gates.	7M	CO1	BL1
2		Explain the parity check and hamming codes with an example.	14M	CO1	BL1
3	a)	Expand the following expression into minterms and maxterms. i). F = B'D+A'D+BD ii) F= (XY+Z) (XZ+Y)	7M	CO2	BL2
	b)	Design combinational circuit by converting Gray code to Binary Code.	7M	CO2	BL3
4		Reduce the following expression in SOP and POS forms using mapping. $f = \Sigma m(0,2,3,10,11,12,13,16,17,18,19,20,21,26,27)$ and implement using NAND logic.	14M	CO2	BL2
5	a)	Design and explain about a SR- Latch using NOR gates in detail, with a neat diagram	7M	CO3	BL3
	b)	What is Race Around Condition? Design clocked master slave JK Flip Flop.	7M	CO3	BL3
6		What is a shift register? Explain about the following modes of operations in a four bit shift register (i) shift right (ii) shift left (iii) bidirectional.	14M	CO3	BL1
7	a)	Design a sequence detector using 110101 sequence.	7M	CO4	BL3
	b)	Discuss about the operation of serial adder with diagram	7M	CO4	BL1
8		Briefly explain the Transistor Transistor Logic (TTL) with an example	14M	CO5	BL1

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