Final: 27-10-2021

Course Code: 1930413 **Roll No:** MLRS- R19

MARRI LAXMAN REDDY
INSTITUTE OF TECHNOLOGY AND MANAGEMENT
(AN AUTONOMOUS INSTITUTION)
(Approved by AICTE, New Delhi & Affiliated to JNTUH, Hyderabad)
Accredited by NBA and NAAC with 'A' Grade & Recognized Under Section2(f) & 12(B)of the UGC act,1956

II B.Tech I Sem Supply End Examination, October 2021

DIGITAL SYSTEM DESIGN

(ECE)

Time: 3 Hours. **Max. Marks: 70**

Note: 1. Answer any FIVE questions.
2. Each question carries 14 marks and may have a, b as sub questions.

1	a)	Design a 3 bit and 4 bit Gray code from 2 bit gray code by reflection.	7M	CO1	BL
	b)	Convert the following: i) AF9.B0D to binary ii) 4796 to hexadecimal.	7M	CO1	BL
2	a)	Realize and draw the following expression using universal gates : A ⊙ B ⊙ C ⊙ D	7M	CO2	BL
	b)	Simplify the function f(A, B, C,D)= A'B'+B'C'+A'D'+CD	7M	CO2	BL
3	a)	Convert the following i) to min-terms: ABC+AB+DC+D' ii) to max terms: A(A'+B)C'	7M	CO2	BL
	b)	Implement the function f(A,B,C,D)=Σ(0,1,4,6,8,9,10,12) using OR-NAND logic gates.	7M	CO3	BL
4	a)	What is Race around condition? How is it achieved in master-Slave Flip Flop?	7M	CO3	BL
	b)	What are the excitation requirements of a flip-flop? Describe for JK and SR flip-flops.	7M	CO3	BL
5	a)	Design a 16:1 MUX using 4:1 MUXs	7M	CO3	BL
	b)	Design an universal shift register of 3 bit using D Flip-Flops.	7M	CO3	BL
6	a)	Design a synchronous 3 bit counter using J K Flip-Flops.	7M	CO4	BL
	b)	Describe the terms with respect to flop-flops i) Clock Skew ii) Propagation delay time	7M	CO4	BL
7	a)	Distinguish between i) asynchronous and synchronous sequential circuits, ii) Mealy and Moor FSM.	7M	CO4	BL
	b)	With the help of a neat circuit diagram and truth table explain the working of DTL NAND gate.	7M	CO5	BL
8	a)	How are the two different IC families interfaced in a design, explain how CMOS logic driving TTL logic.	7M	CO5	BL
	b)	Analyze the characteristics of standard TTL NAND gate.	7M	CO5	BL

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