Course Code: 1931213 **Roll No:** **MLRS- R19**

MARRI LAXMAN REDDY
INSTITUTE OF TECHNOLOGY AND MANAGEMENT
(AN AUTONOMOUS INSTITUTION)
(Approved by AICTE, New Delhi & Affiliated to JNTUH, Hyderabad)
Accredited by NBA and NAAC with 'A' Grade & Recognized Under Section2(f) & 12(B)of the UGC act,1956

II B.Tech I Sem Supplementary Examination, February-2022

Computer Organization and Microprocessor

(IT)

Time: 3 Hours. **Max. Marks: 70**

Note: 1. Answer any FIVE questions.
2. Each question carries 14 marks and may have a, b as sub questions.

1	a)	List out the memory reference instructions and interpret each instruction in detail.	7M	CO1	BL-2
	b)	Show the control unit of a basic computer and discuss the components.	7M	CO1	BL-2
2		Inspect the address sequencing capabilities required in a control memory and demonstrate the mechanism required for selection of the address for control memory.	14M	CO1	BL-4
3	a)	Assess any seven various addressing modes with syntax and examples.	7M	CO2	BL-3
	b)	State and explain the general formats of different instructions in 8086 instruction set.	7M	CO2	BL-2
4		Outline the architecture of 8086 processor and describe the register organization of 8086 processor in detail.	14M	CO2	BL-2
5	a)	Write a program to add a data byte located at offset 0500H in 2000H segment to another data byte available at 0600H in the same segment and store the result at 0700H in the same segment.	7M	CO3	BL-3
	b)	Summarize the advantages of assembly language over machine language and lit out the disadvantages of machine level programming.	7M	CO3	BL-2
6		Demonstrate the complete procedure for programming with an assembler with suitable example.	14M	CO3	BL-2
7	a)	Design the flowchart for addition and subtraction operation of signed- magnitude numbers.	7M	CO4	BL-3
	b)	Illustrate the procedure for the asynchronous data transfer between two independent units.	7M	CO4	BL-2
8		Define the cache memory. Analyze various types of mapping procedures when considering the organization of cache memory.	14M	CO5	BL-4

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