



II B. Tech II Sem Regular End Examination, August 2021

LINEAR IC APPLICATIONS**(ECE)****Time: 3 Hours.****Max. Marks: 70**

Note: 1. Answer any FIVE questions.

2. Each question carries 14 marks and may have a, b as sub questions.

- | | | | | | |
|---|----|---|----|-----|----|
| 1 | a) | List DC and AC Characteristics of an Op-Amp. | 7M | C01 | L1 |
| | b) | Draw the equivalent circuit of an ideal Op-Amp and explain. | 7M | C01 | L3 |
| 2 | a) | Explain about input offset voltage with neat diagram. | 7M | C01 | L2 |
| | b) | Define slew rate and how it affects Op-Amp performance and explain. | 7M | C01 | L1 |
| 3 | a) | How Op-amp acts as an Integrator and Differentiator? | 7M | C02 | L1 |
| | b) | Explain Schmitt Trigger in detail using 741 Op-amp. | 7M | C02 | L1 |
| 4 | a) | Explain about the Instrumentation Amplifier. | 7M | C02 | L1 |
| | b) | With a neat diagram explain low pass filter and derive the expression for output voltage. | 7M | C03 | L3 |
| 5 | a) | Design a first order band pass filter with lower cutoff frequency of 100Hz and a higher cutoff frequency of 1KHz. The pass band gain should be 4. Calculate the 'Q' of the filter | 7M | C03 | L4 |
| | b) | Draw the wide band reject filter circuit and also the frequency response of it. | 7M | C03 | L4 |
| 6 | a) | Explain block diagram of PLL emphasizing the capture range and lock in range | 7M | C04 | L1 |
| | b) | Design Monostable Multivibrator using 555 timer to produce pulse width of 100 m sec | 7M | C04 | L3 |
| 7 | a) | Draw the block diagram of 555 timer and explain function of each pin of 555 timer | 7M | C04 | L4 |
| | b) | With neat sketch explain the operation of Dual slope ADC. | 7M | C05 | L3 |
| 8 | a) | In Detail how the digital information converted to analog by using 4 bit binary weighted resistor method | 7M | C05 | L3 |
| | b) | Draw and Explain the circuit operation of successive approximation of ADC | 7M | C05 | L3 |