

Course Code: 1950404

Roll No:

MLRS- R19



**MARRI LAXMAN REDDY
INSTITUTE OF TECHNOLOGY AND MANAGEMENT**

(AN AUTONOMOUS INSTITUTION)

(Approved by AICTE, New Delhi & Affiliated to JNTUH, Hyderabad)

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III B.Tech I Sem Regular End Examination, January 2022

Microprocessors and Microcontrollers

(ECE)

Time: 3 Hours.

Max. Marks: 70

Note: 1. Question paper consists: Part-A and Part-B.

2. In Part - A, answer all questions which carries 20 marks.

3. In Part - B, answer any one question from each unit.

Each question carries 10 marks and may have a, b as sub questions.

PART- A

(10*2 Marks = 20 Marks)

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|-------|---------------------------------------------------------------------------------------------------------------|----|-----|-----|
| 1. a) | Describe the procedure used in 8086 processor to generate the physical address. | 2M | C01 | BL2 |
| b) | Give an example each of Relative Based Indexed and Intra segment indirect addressing modes of 8086 processor. | 2M | C01 | BL1 |
| c) | What is the difference between MOVC and MOVX instructions in 8051 microcontroller? | 2M | C02 | BL1 |
| d) | List out the hardware interrupts of 8051 microcontroller, give their order of priority. | 2M | C02 | BL1 |
| e) | Draw a block diagram showing the interface of common 7 segment display to 8051 microcontroller. | 2M | C03 | BL1 |
| f) | What are the initialization steps by I2C bus interface in a system? | 2M | C03 | BL1 |
| g) | What is the meaning of ARM is a LOAD-STORE architecture? | 2M | C04 | BL1 |
| h) | List out the stack instructions in ARM processor. | 2M | C04 | BL1 |
| i) | How does nested vectored interrupt controller (NVIC) work in CORTEX M3 processor? | 2M | C05 | BL2 |
| j) | Which two cores are merged to get OMAP processor? | 2M | C05 | BL1 |

PART- B

(10*5 Marks = 50 Marks)

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|------|-----------------------------------------------------------------------------------------|----|-----|-----|
| 2 a) | Briefly describe the architectural features of 8086 microprocessor. | 5M | C01 | BL2 |
| b) | Write an assembly language program to search for a number in a given string of numbers. | 5M | C01 | BL3 |

OR

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| 3 | With the help of a neat timing diagrams explain the READ and WRITE cycles in minimum mode of 8086 microprocessor. | 10M | C01 | BL2 |
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| 4 | a) | List out the addressing modes of 8051 instructions with an example each. | 5M | C02 | BL2 |
| | b) | Write an assembly language program to perform arithmetic and logical operations using 8051. | 5M | C02 | BL3 |
| OR | | | | | |
| 5 | | Describe the Timer/ Counter operation of 8051 in all modes. | 10M | C02 | BL2 |
| 6 | a) | Interface 16K Byte memory to 8051 as external memory. Give the memory map for the same. | 5M | C03 | BL3 |
| | b) | List out the pins of RS-232 and describe the function of each one of them. | 5M | C03 | BL2 |
| OR | | | | | |
| 7 | | Investigate the I/O ports operations in 8051 with neat sketch. | 10M | C03 | BL5 |
| 8 | a) | Describe the programmer model of ARM processor. | 5M | C04 | BL2 |
| | b) | How does ARM processor handle instruction pipeline? | 5M | C04 | BL2 |
| OR | | | | | |
| 9 | | Describe multiple register load-store instructions with ARM Processor. | 10M | C04 | BL2 |
| 10 | a) | How is memory protection unit function in ARM CORTEX M3? | 5M | C05 | BL2 |
| | b) | List out the registers of OMAP processors. | 5M | C05 | BL2 |
| OR | | | | | |
| 11 | | Draw and explain ARM CORTEX M3 processor architecture. | 10M | C05 | BL4 |

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