Course Code: 1960421 Roll No: MLRS-R19

MARRI LAXMAN REDDY
INSTITUTE OF TECHNOLOGY AND MANAGEMENT
(AN AUTONOMOUS INSTITUTION)
(Approved by AICTE, New Delhi & Affiliated to JNTUH, Hyderabad)
Accredited by NBA and NAAC with 'A' Grade & Recognized Under Section2(f) & 12(B)of the UGC act,1956

III B.Tech II Sem Regular End Examination, June 2022

VLSI Design

(Electronics and Communication Engineering)

Time: 3 Hours. **Max. Marks: 70**

Note: 1. Question paper consists: Part-A and Part-B.
2. In Part – A, answer all questions which carries 20 marks.
3. In Part – B, answer any one question from each unit.
Each question carries 10 marks and may have a, b as sub questions.

PART- A

(10*2 Marks = 20 Marks)

1.	a)	Define transconductance and figure of merit	2M	CO1	BL1
	b)	Explain about the CMOS inverter	2M	CO1	BL4
	c)	What are the different MOS layers?	2M	CO2	BL1
	d)	Differentiate two scaling techniques.	2M	CO2	BL2
	e)	Define time delay	2M	CO3	BL1
	f)	Define fan in and fan out	2M	CO3	BL1
	g)	What is pipelining?	2M	CO4	BL1
	h)	Write about the Serial Access Memories	2M	CO4	BL1
	i)	Write any two Test Principles	2M	CO5	BL1
	j)	List the applications of FPGA.	2M	CO5	BL1

PART- B

(10*5 Marks = 50 Marks)

2	a)	Explain the nMOS enhancement mode fabrication process	5M	CO1	BL4
	b)	Compare CMOS and Bipolar technologies.	5M	CO1	BL2
		OR			
3		With neat sketches explain the CMOS n-well fabrication process.	10M	CO1	BL4
4	a)	Explain about CMOS lambda based design rules.	5M	CO2	BL4
	b)	Draw and explain about BICMOS inverter.	5M	CO2	BL4
		OR			
5		Design a stick diagram for two input CMOS NAND and NOR gates?	10M	CO2	BL6

6	a)	Design XOR gate with CMOS	5M	CO3	BL6
	b)	Explain about the Driving large capacitive loads	5M	CO3	BL4
		OR			
7		Design NAND and NOR using CMOS	10M	CO3	BL6
8	a)	Explain about the ALU	5M	CO4	BL4
	b)	Write in detail about the adders	5M	CO4	BL1
		OR			
9		Difference between SRAM and DRAM	10M	CO4	BL2
10	a)	Draw the typical architecture of PLA and PAL	5M	CO5	BL1
	b)	Difference between PLD and CPLD	5M	CO5	BL2
		OR			
11		Explain about the Chip level Test Techniques.	10M	CO5	BL4

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