Course Code: 2030504 Roll No: **MLRS- R20**

MARRI LAXMAN REDDY
INSTITUTE OF TECHNOLOGY AND MANAGEMENT
(AN AUTONOMOUS INSTITUTION)
(Approved by AICTE, New Delhi & Affiliated to JNTUH, Hyderabad)
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II B.Tech I Sem Supply End Examination, July-2022

Digital Logic Design

(CSE, CSI & IT)

Max. Marks: 70

Note: 1. Question paper consists: Part-A and Part-B.
2. In Part – A, answer all questions which carries 20 marks.
3. In Part – B, answer any one question from each unit.
Each question carries 10 marks and may have a, b as sub questions.

PART- A

(10*2 Marks = 20 Marks)

1.	a)	Given that $(16)_{10}=(100)_b$, determine the value of b.	2M	CO1	BL2
	b)	Given binary numbers a=1010.11 , b=1001.01 perform the a * b binary operation.	2M	CO1	BL2
	c)	How the multiple variable exclusive OR operation is defined as an odd function?	2M	CO2	BL2
	d)	What is the significance of don't care conditions in k-map?	2M	CO2	BL2
	e)	Draw the diagram of two-to-one-line multiplexer with three-state buffers.	2M	CO3	BL1
	f)	What are the symbols used for logic AND and logic OR in Verilog HDL?	2M	CO3	BL1
	g)	Draw the block diagram of sequential circuit.	2M	CO4	BL1
	h)	Write characteristic table for JK flip-flop.	2M	CO4	BL1
	i)	Compare PAL and PLA.	2M	CO5	BL2
	j)	What is mean by non-critical race?	2M	CO5	BL1

PART- B

(10*5 Marks = 50 Marks)

2	a)	The following arithmetic operations is correct in at least one number system. Determine the possible bases of the numbers in each operation. 41/3=13	5M	CO1	BL3
	b)	How a register can store any discrete quantity of information and how the information transfer among the registers?	5M	CO1	BL3

OR

3	(i)	Write the following Boolean express in sum of products form: (b+d)(a'+b'+c)	10M	CO1	BL3
	(ii)	Reduce the Boolean expression to the two literals ABC'D+A'BD+ABCD			
	(iii)	Find the complement of the function z+z'(v'w+xy)			

4	a)	Implement the following Boolean function with NAND gates: $F(x,y,z)=\sum(1,2,3,4,5,7)$	5M	CO2	BL4
	b)	Write the general procedure for converting a multilevel AND-OR diagram into all NAND diagram using mixed notations.	5M	CO2	BL3

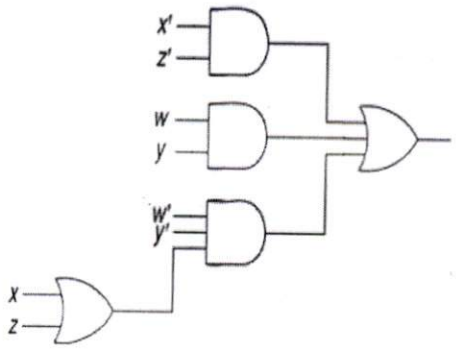
OR

5	Use the map method to simplify the following function and draw the logic diagram: $f(v,w,x,y,z) = \sum(0,1,2,4,5,9,11,13,15,16,18,22,23,26,29,30,31)$	10M	CO2	BL5
6 a)	Draw the logic diagram of two bit by two bit multiplier and explain its multiplication process.	5M	CO3	BL3
b)	Write the HDL program for two-to-four line decoder.	5M	CO3	BL3
	OR			
7	Design a four bit adder-subtractor with over flow detection and draw its logic diagram and also explain its working with example.	10M	CO3	BL4
8 a)	Draw the block diagrams of Mealy and Moore state machines and compare them.	5M	CO4	BL3
b)	Design a three bit binary counter and draw its logic diagram.	5M	CO4	BL4
	OR			
9	For the following state table	10M	CO4	BL4

Present State	Next State		output	
	X=0	X=1	X=0	X=1
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

(i) Draw the corresponding state diagram.
(ii) Tabulate the reduced state table.
(iii) Draw the state diagram corresponding to the reduced state table.

10 a)	A 12-bit Hamming code word containing 8 bits of data and 4 parity bits is read from memory. What was the original 8 bit data word that was written into memory if the 12-bit word read out as 101110000110	5M	CO5	BL4
b)	Tabulate the PLA programming table for the four Boolean functions listed below. Minimize the number of product terms. A(x,y,z)= Σ(1,3,5,6) B(x,y,z)=Σ(0,1,6,7) C(x,y,z)=Σ(3,5)	5M	CO5	BL3
	OR			
11	Analyze the circuit shown below for SIC static hazards. Redesign it to make it SIC hazard free.	10M	CO5	BL5



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