



III B.Tech I Sem Regular End Examination, December 2022

Linear and Digital IC Applications

(ECE)

Time: 3 Hours.**Max. Marks: 70**

Note: 1. Question paper consists: Part-A and Part-B.

2. In Part – A, answer all questions which carries 20 marks.

3. In Part – B, answer any one question from each unit.

Each question carries 10 marks and may have a, b as sub questions.

PART- A**(10*2 Marks = 20 Marks)**

1.	a)	The two input terminals of an Op-AMP are known as	2M	C01	BL
	b)	The output voltage of a particular op-amp increases 8 V in 12 μ s in response to step on the input. The slew rate is----	2M	C01	BL
	c)	Draw the block schematic of PLL.	2M	C02	BL
	d)	What are the advantages of active filters over passive filters?	2M	C02	BL
	e)	What are the types of ADC?	2M	C03	BL
	f)	Define resolution of a DAC.	2M	C03	BL
	g)	Sketch the logic levels for typical CMOS logic circuits.	2M	C04	BL
	h)	Compare decoder and demultiplexer.	2M	C04	BL
	i)	Explain about tristate logic in TTL.	2M	C05	BL
	j)	Compare latch and flip flop.	2M	C05	BL

PART- B**(10*5 Marks = 50 Marks)**

2	a)	Explain with diagram, the working of an inverting amplifier circuit. Obtain the equation for its gain.	5M	C01	BL
	b)	Define the following terms: (i) Slew Rate. (ii) Thermal drift.	5M	C01	BL
OR					
3	a)	Draw and explain the operation of current to voltage converter	5M	C01	BL
	b)	Explain with diagram, the instrumentation amplifier circuit and its applications.	5M	C01	BL
4	a)	Draw the circuit diagram of second order low pass filter and explain its operation.	5M	C02	BL
	b)	With a neat sketch, explain the operation of Quadrature oscillator.	5M	C02	BL
OR					

5	a)	Explain the working of a monostable multivibrator using 555 timer.	5M	C02	BL
	b)	Draw the block diagram of a PLL and mention the function of each block	5M	C02	BL
OR					
6	a)	With a neat diagram, explain working of weighted resistor DAC.	5M	C03	BL
	b)	Explain the working of a dual slope A to D converter	5M	C03	BL
OR					
7	a)	Explain in detail about specifications of DAC.	5M	C03	BL
	b)	Explain the working of a Flash type A to D converter	5M	C03	BL
OR					
8	a)	Implement full adder with 4 to 1 multiplexer.	5M	C04	BL
	b)	Implement 64 x 1 multiplexer with four 16 x 1 and one 4 x 1 multiplexer.	5M	C04	BL
OR					
9	a)	With a neat circuit diagram explain the analysis and characteristics of standard TTL NAND gate.	5M	C04	BL
	b)	Give the comparison of various logic families.	5M	C04	BL
OR					
10	a)	Draw and explain 4-bit universal shift register.	5M	C05	BL
	b)	Explain the differences between asynchronous and synchronous counters. Design a MOD-6 ripple counter.	5M	C05	BL
OR					
11	a)	Explain about RAM architecture.	5M	C05	BL
	b)	Explain about types of RAMS.	5M	C05	BL

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CO - Course Outcome**BL - Blooms Taxonomy Levels**

Note: 1. Font style: Cambria.

2. Bloom's Taxonomy Level (BL) shall be mentioned for each question.