COURSE CONTENT

DIGITAL LOGIC DESIGN LABORATORY								
III Semester: ECE								
Course Code	**Category**	**Hours/ Week**			**Credits**	**Maximum Marks**		
2530473	**Core**	**L**	**T**	**P**	**C**	**CIA**	**SEE**	**Total**
		0	**0**	**2**	**1**	**40**	**60**	**100**
Contact Classes: Nill	**Tutorial Classes: Nil**	**Practical Classes: 32**				**Total Classes:32**		
Prerequisites: Nill								

Couse Overview:

This laboratory course offers practical experience in designing, analysing, and simulating digital circuits. Students start with basic hardware implementation using logic gate ICs, covering Boolean simplification, arithmetic circuits, code converters, and other combinational modules. The course then progresses to Verilog HDL-based design, introducing dataflow, behavioural, and structural modelling with simulation tools. Emphasis is placed on strengthening core logic concepts while developing skills for modern digital system design.

Course Objectives:

The students will try to learn

- Practical skills in analysing and simplifying Boolean expressions.
- Hands-on experience in designing combinational and sequential logic circuits.
- Digital system modelling using Verilog HDL.
- Simulating and verifying designs with EDA tools.
- Construction of modular digital systems such as counters, FSMs, and shift registers.

Course Outcomes:

After successful completion of the course, students shall be able to

- Analyse and simplify Boolean expressions and implement them using logic gates and ICs.
- Design and realize combinational and sequential logic circuits using logic gate hardware.
- Model digital systems in Verilog HDL using dataflow, behavioural, and structural styles.
- Simulate and verify digital designs using industry-standard EDA tools and testbenches.
- Build modular and hierarchical designs such as counters, FSMs, and shift registers.

List of Experiments:

A. Realization in Hardware Laboratory (Using Logic ICs)

These are fundamental hands-on experiments conducted using logic ICs such as AND, OR, NOT, NAND, NOR, XOR gates, flip-flops, multiplexers, and decoders.

1. Realize and minimize Boolean functions using basic gates and universal gates (NAND/NOR) in SOP/POS form.
2. Design and implement Half Adder, Full Adder using logic gates.
3. Design and implement Half Subtractor, and Full Subtractor using logic gates.
4. Construct and analyse basic logic gates (AND, OR, NOT, XOR, XNOR) using only NAND and NOR gates.
5. Design and implement code converters such as Binary to Gray, Gray to Binary, using gates.
6. Design and implement simple combinational circuits: 2-to-1 multiplexer, 1-bit comparator

B. Verilog HDL-Based Digital Design Experiments (Simulation-Based)

These experiments are implemented using Verilog HDL with different modelling styles (dataflow, behavioural, structural) and simulated using tools like Vivado/Model Sim/Xilinx ISE/cadence/ any equivalent.

1. Design and simulate a 2-bit comparator using dataflow modelling; extend it to 4-bit using structural modelling.
2. Implement a 2:1 multiplexer using dataflow modelling and design an 8:1 multiplexer using structural modelling.
3. Design a 2-to-4 decoder using dataflow modelling and realize a 3-to-8 decoder using structural modelling.
4. Implement a given Boolean function using a decoder-based approach in behavioural modelling.
5. Design and simulate a universal n-bit shift register (left, right, hold, parallel load) using behavioural modelling.
6. Design a synchronous MOD-n counter using behavioural modelling with D or JK flip-flops.
7. Design and simulate an asynchronous (ripple) counter for a custom sequence using structural modelling.
8. Implement a sequence detector for a given binary pattern using FSM (Moore/Mealy) in behavioural modelling.

Open Ended Experiments

a. Implementation of binary multiplier
b. Design and simulation of Registers
c. Implementation of binary counter and simulate using simulation tool

NOTE: Minimum 5 experiments from each PART to be conducted.

Reference Link

1. https://onlinecourses.nptel.ac.in/noc25_cs25/preview
2. https://nptel.ac.in/courses/106103358
3. https://www.nptelprep.in/courses/106103358
4. https://onlinecourses.nptel.ac.in/noc25_ee180/preview
5. https://onlinecourses.nptel.ac.in/noc26_ee71/preview
6. https://onlinecourses-archive.nptel.ac.in/noc18_cs30
7. https://onlinecourses-archive.nptel.ac.in/noc18_cs48/course

Materials Online:

1. Lab Manual
2. Open-ended experiments